

In the Claims:

Claims 1-13 (Canceled)

14. (currently amended) A semiconductor device, comprising:

a substrate having a first conductivity type;

a buried layer of a second conductivity type disposed in a top portion of said substrate;

an epitaxial layer of the first conductivity type disposed over said buried layer;

a lateral double-diffused metal oxide semiconductor (LDMOS) device disposed in the substrate, the LDMOS device including a drain;

a first guard ring disposed around and proximate the drain of the LDMOS device; and

a second guard ring disposed around the first guard ring.

15. (original) The method according to Claim 14, wherein the first guard ring and the second guard ring comprise a semiconductive material.

16. (original) The semiconductor device according to Claim 14, wherein the first guard ring comprises a P+ base guard ring, and wherein the second guard ring comprises an N+ collector guard ring.

17. (original) The semiconductor device according to Claim 16, wherein the first guard ring and second guard ring form a parasitic transistor, wherein the parasitic transistor electrically isolates the drain of the LDMOS

18. (currently amended) The semiconductor device according to Claim 14, wherein the buried and epitaxial layers disposed within the semiconductor ~~comprises~~ comprise an N+ buried layer

formed in a top portion of the substrate, and a P-epitaxial layer disposed over the N+ buried layer.

19. (original) The semiconductor device according to Claim 18, wherein the P-epitaxial layer comprises about 9-10 μm of doped semiconductor material.

20. (original) The semiconductor device according to Claim 18, further comprising a deep N-well formed within the P-epitaxial layer, wherein the first or second guard ring is formed in the deep N-well.

21. (original) The semiconductor device according to Claim 20, wherein the deep N-well comprises the entire thickness of the P-epitaxial layer.

22. (original) A lateral double-diffused metal oxide semiconductor (LDMOS) device, comprising:

a substrate, the substrate comprising a first semiconductor type;

a buried layer formed in a top region of the substrate, the buried layer comprising a second semiconductor type;

a doped semiconductor material disposed over the buried layer, the doped semiconductor material being doped with the first semiconductor type;

a deep well region disposed within a portion of the doped semiconductor material, the deep well region comprising an annular ring shape and being doped with the first semiconductor type;

at least one first high voltage well region formed within a portion of the doped semiconductor material;

a second high voltage well region formed within a portion of the doped semiconductor

material, the second high voltage well region comprising an annular shape disposed within a central portion of the annular deep well region;

field dielectric disposed over portions of the at least one first high voltage well region and the second high voltage well region;

a gate dielectric disposed over portions of the at least one first high voltage well region, the second high voltage well region, and a portion of the field dielectric;

a gate of the LDMOS device disposed over the gate dielectric;

a source of the LDMOS device formed in the second high voltage well region;

a drain of the LDMOS device formed in the at least one first high voltage well region;

a first guard ring formed in the annular deep well region; and

a second guard ring formed in the second high voltage well region, the second guard ring being formed in a central region of the first guard ring.

23. (original) The LDMOS device according to Claim 22, wherein the first semiconductor type comprises P-type, wherein the second semiconductor type comprises N+, wherein the deep well region comprises an N-well, wherein the at least one first high voltage well region comprises a high voltage N-well (HVNW) region; wherein the second high voltage well region comprises a high voltage P well (HVPW) region; wherein the dopant of the second semiconductor type comprises N+, and wherein the dopant of the first semiconductor type comprises P+.

24. (original) The LDMOS device according to Claim 22, wherein the P-doped semiconductor material comprises about 9-10 μm of P-epitaxial doped semiconductor material.

25. (original) The LDMOS device according to Claim 22, wherein the deep N-well region comprises the entire thickness of the P-doped semiconductor material.

26. (original) The LDMOS device according to Claim 22, wherein the field dielectric comprises a field oxide, and wherein the gate dielectric comprises a gate oxide.